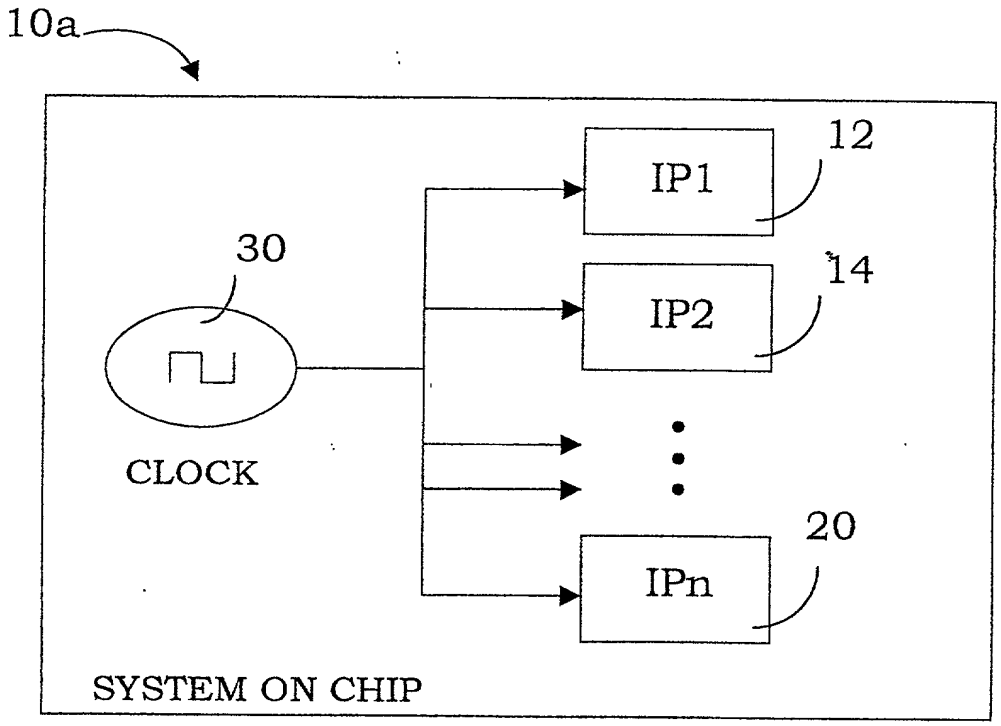
10a
12
IP1
30
14
IP2
CLOCK
20
IPn
SYSTEM ON CHIP

FIG. 1

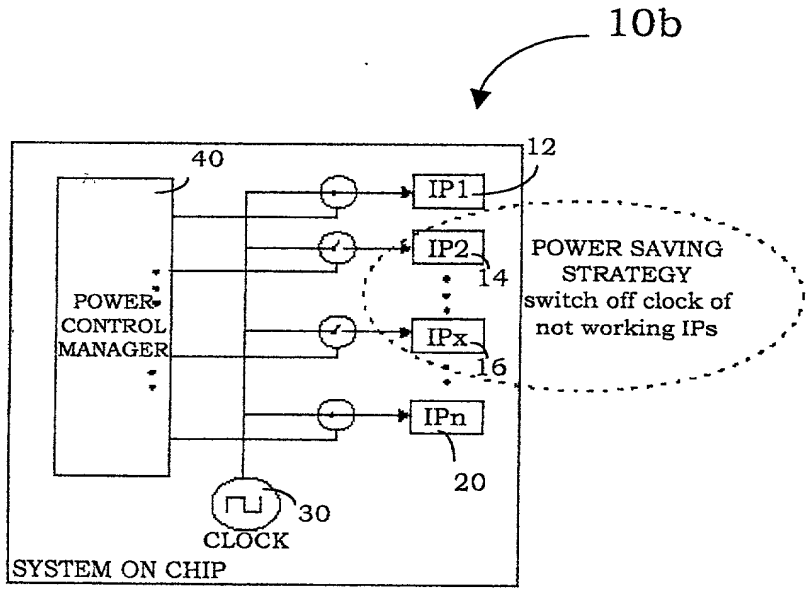
10b
40
12
IP1
IP2
14
POWER SAVING
STRATEGY
switch off clock of
not working IPs
POWER
CONTROL
MANAGER
IPx
16
IPn
20
30
CLOCK
SYSTEM ON CHIP

FIG. 2

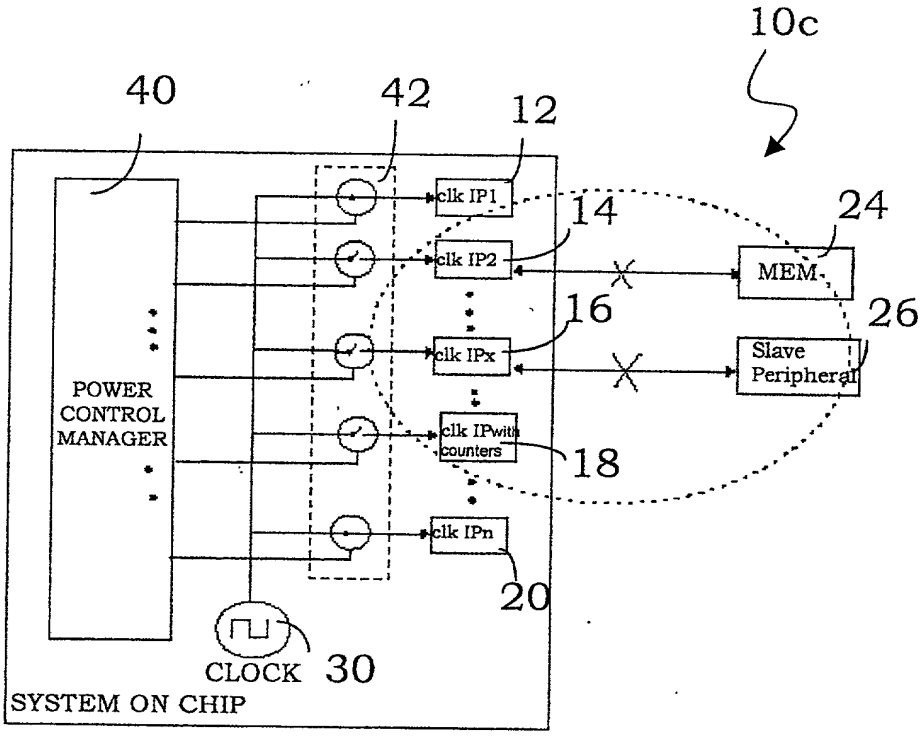
10c
40
42
12
clk IP1
14
clk IP2
24
MEM
16
clk IPx
26
Slave Peripheral
POWER CONTROL MANAGER
clk IPwith counters
18
clk IPn
20
CLOCK
30
SYSTEM ON CHIP

FIG. 3

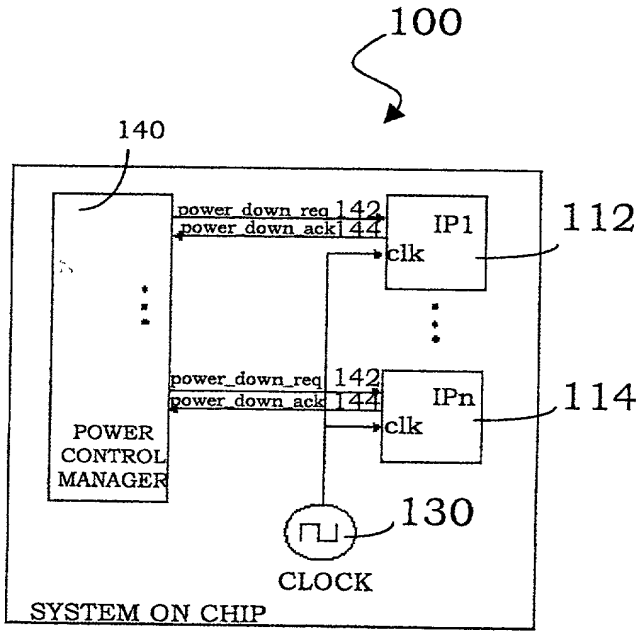
100
140
power_down_req 142
power_down_ack 144
IP1
112
clk
power_down_req 142
power_down_ack 144
IPn
114
clk
POWER CONTROL MANAGER
130
CLOCK
SYSTEM ON CHIP

FIG. 4

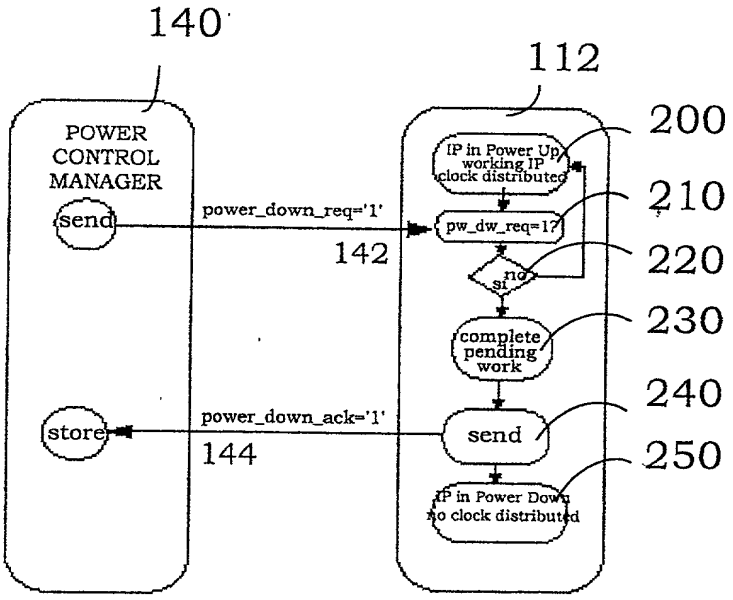

FIG. 5

190

```
Power Down Manager:
        sent to the IP the power_down_req signal set to '1';

IP:
        IF power_down_req is asserted (='1'):
                    complete its pending work;
                    set power_down_ack to '1';
                    stop its own clock => IP halted;
        else
                    normal work;

Power Down Manager:
        Stores the value of power_down_ack to allow visibility
        of IP status (power on/off);
```

FIG. 6

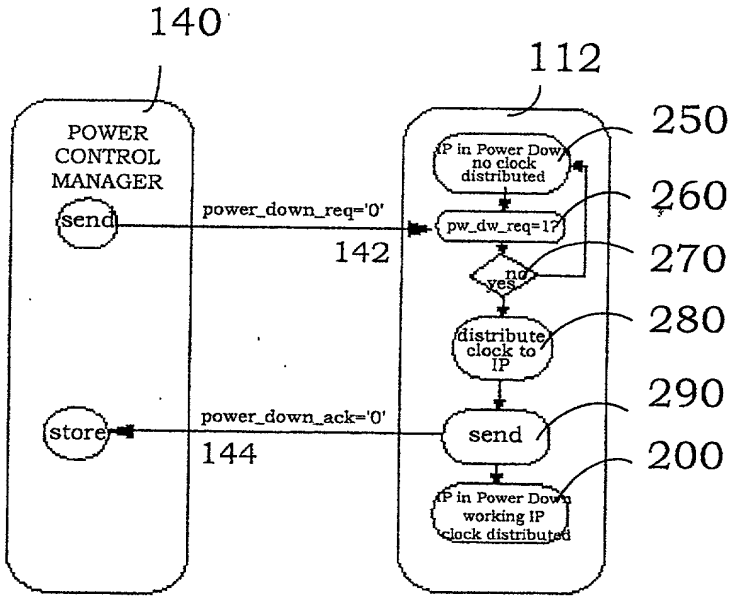

FIG. 7

194

```
Power Down Manager:
        sent to the IP the power_down_req signal set to '0';

IP:
        IF power_down_req is de_asserted (='0'):
                    restarts its own clock;
                    set power_down_ack = '0';
                    restart to work;
        else
                    no clock distributed to IP => IP halted;

Power Down Manager:
        Stores the value of power_down_ack to allow visibility
        of IP status (power on/off);
```

FIG. 8

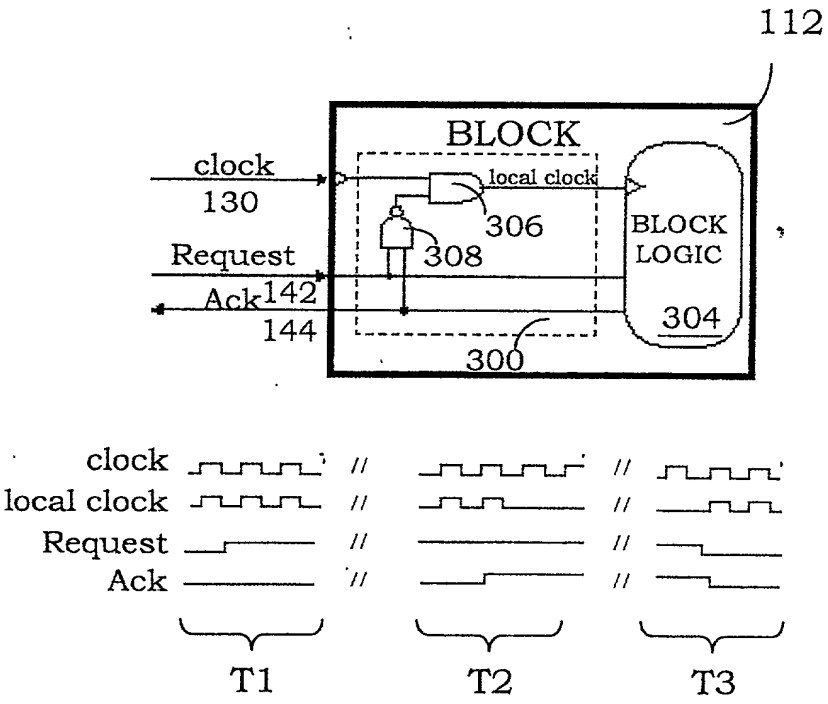
112
BLOCK
clock
130
local clock
306
308
Request
Ack
142
144
BLOCK
LOGIC
304
300
clock
local clock
Request
Ack
T1
T2
T3

FIG. 9

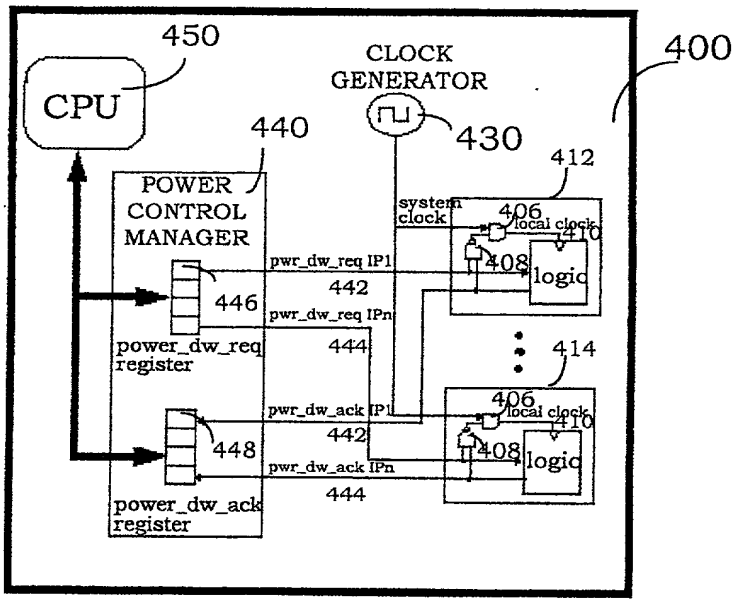
450
CPU
CLOCK
GENERATOR
400
440
430
412
POWER
CONTROL
MANAGER
system
clock
406
local clock
410
408
logic
pwr_dw_req IP1
442
446
pwr_dw_req IPn
power_dw_req
register
444
414
406
local clock
410
pwr_dw_ack IP1
442
448
408
logic
pwr_dw_ack IPn
444
power_dw_ack
register

FIG. 10